REMARKS/ARGUMENTS

In this Application, Claims 1-23 are pending. Claim 24 was previously canceled. Claim 1, 12, and 23 are amended, and no claims are canceled or newly presented in this response.

I. TECHNICAL CORRECTIONS TO SPECIFICATION AND ABSTRACT

A few paragraphs in the specification and the abstract have been amended to correct minor typographical errors. No new matter is added hereby.

II. TECHNICAL AMENDMENTS TO CLAIM

Claims 1 and 23 have been amended to ensure proper antecedent bases. These amendments are merely to ensure compliance with statutory formalities and are not intended as, and should not be construed as, limiting or narrowing amendments.

III. CLAIM OBJECTIONS

Claim 12 was objected to because claim 12 recited "in anyone of claim 1." Applicant thanks the Examiner for pointing this out and has amended the claim accordingly.

IV. CLAIM REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-2 are rejected under 35 U.S.C. § 102(b) as being anticipated by Day (EP 0893767) (hereinafter "Day").

The Office Action asserts that Day discloses each said non-configured module including counter means which is incremented each time a non-configured module is configured, said counter [means] of each non-configured module, once configured, providing a unique code which is indicative of the position of the module in the system. Applicant respectfully disagrees.

While Day is directed to a Master/Slave serial bus which allows addresses of circuit boards/modules on a bus to be determined upon bus power up, Day fails to disclose "each said non-configured module including counter means," or "counter means which is incremented each time a non-configured module is configured," or that "said counter means . . . provid[es] a unique code which is indicative of the position of the module in the system" (emphases added) as recited in claim 1. In fact, Day teaches away from the above by teaching that each unique software address for each slave circuit board is "assigned" and that Assign Address commands from the bus master assign a unique software address to each circuit board (Day col. 3, lines 42-

48). That is, instead of using a counter means included in each non-configured module, Day uses an Assign Address command from the master to assign an address.

Using counter means, such as a simple counter, is naturally an inexpensive and elegant solution to addressing modules on a LIN bus at power up. Also, using a simple counter in each module avoids the need for excess software/firmware code in the master bus controller. Neither Day nor the other relied upon reference, De Haas et al. (US 6,664,821), teaches or suggests such a solution; thus, the claim distinguishes over the relied-upon references. For at least the reasons above, Applicant respectfully requests withdrawal of the rejection of independent claim 1 as well as claim 2 which depends thereon.

V. CLAIM REJECTIONS UNDER 35 U.S.C. § 103

Claims 3-4, 6-9, 11, and 13-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable (obvious) over Day in view of De Haas et al. (US 6,664,821) (hereinafter, "De Haas"). Claims 10 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable (obvious) over Day in view of De Haas and further in view of the Examiner's Official Notice that a unique software address could be generated by a random code generator. Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable (obvious) over Day in view of De Haas and further in view of another Examiner's Official Notice that it would be obvious to try a resister value of 1 ohm.

Each of the claims depending from claim 1 is patentably distinguished from the combined teachings of Day and De Haas by at least the novel limitation discussed in the section above. Note again that the primary reference, Day, teaches away from the invention as claimed. As such, claim 1 and dependent claims 2-22 of the present invention are novel and nonobvious with respect to Day in view of De Haas.

Notwithstanding the above, claim 4 of the present application is further distinguished over the combination of Day and De Haas by the limitation that "said reconfigurable module has two LIN Bus interface pins connected by a series resister." This is not disclosed or suggested in De Haas which merely describes the connection of multiple slave notes (SLV) connected to a single LIN Bus wire (LB). The resistor referred to in the Office Action at page 6 (Resistor R1 of De Haas FIG. 2) is akin to the pull-up resistor 104 of the

exemplary embodiment in FIG. 1 of the present application, and not series resistor 103. Thus, De Haas does not teach or suggest the required structure. As for the other relied-upon reference, Day does not explicitly disclose a LIN Bus as acknowledged in the Office Action (Office Action p. 5). Therefore, claim 4 is novel and inventive over the teachings of Day and De Haas.

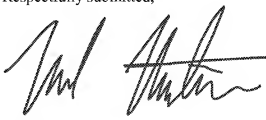
As is the case with independent claim 1, independent claim 23 is patentably distinguished over Day by the limitation of "incrementing a position counter of each module . . . the position counters for each module thus showing a value associated with a unique position in the chain." As discussed above, this limitation is not disclosed or suggested by the relied upon references, and therefore the claim distinguishes over the cited references. Applicant therefore respectfully requests withdrawal of the rejection.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 925-472-5000.

Respectfully submitted,



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